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DOCUMENT-IDENTIFIER: US 6174796 B1
TITLE: Semiconductor device manufacturing method

Abstract Text (1):
A semiconductor device manufacturing method having a copper wiring, comprises the steps of forming a second insulating film for covering the wiring on a first insulating film, forming a third insulating film which is made of material different from the second insulating film on the second insulating film, coating a resist on the third insulating film and then forming an opening over the wiring by exposing and developing the resist, forming a hole or groove in the third insulating film by etching the third insulating film via the opening, removing the resist by placing the semiconductor substrate in a plasma atmosphere containing oxygen in a chamber and simultaneously removing a part of the second insulating film via the hole or groove to expose the wiring via the hole or groove, and forming a metal film in the hole or groove.

Brief Summary Text (21):
In order to achieve the above object, according to an aspect of the present invention, there is provided a semiconductor device manufacturing method comprising the steps of forming a wiring on a first insulating film which is formed on a semiconductor substrate, forming a second insulating film for covering the wiring, forming a third insulating film which is made of material different from the second insulating film on the second insulating film, coating a resist on the third insulating film and then forming an opening over the wiring by exposing and developing the resist, forming a hole or groove in the third insulating film by etching the third insulating film via the opening by virtue of a reactive ion etching method, removing the resist, forming an inclined surface by etching an upper edge portion of the third insulating film around the hole or groove to thus extend an upper portion of the hole or groove, removing a part of the second insulating film via the hole or groove by the reactive ion etching method, and forming a metal film in the hole or groove.

Brief Summary Text (26):
According to an aspect of the present invention, there is provided a semiconductor device manufacturing method comprising the steps of forming a wiring on a first insulating film which is formed on a semiconductor substrate, forming a second insulating film for covering the wiring, forming a third insulating film which is made of material different from the second insulating film on the second insulating film, coating a resist on the third insulating film and then forming an opening over the wiring by exposing and developing the resist, forming a hole or groove in the third insulating film

by etching the third insulating film via the opening, removing the resist by placing the semiconductor substrate in a plasma atmosphere containing oxygen in a chamber and simultaneously removing a part of the second insulating film via the hole or groove to expose the wiring via the hole or groove, and forming a metal film in the hole or groove.

Brief Summary Text (27):
According to another invention, removal of the resist being employed in forming the hole or groove and removal of the second insulating film via the hole or groove are executed simultaneously by using the oxygen containing plasma. For this reason, since the wiring is exposed to the oxygen plasma in etching the second insulating film, such wiring becomes difficult to be etched because the surface of the second wiring is oxidized. As a result, sticking of the metal of the wiring onto the side wall becomes difficult.

Detailed Description Text (9):
A resist 8 is coated on the interlayer insulating film 7 to a thickness of 0.7 .mu.m. A via opening portion 8a of a diameter of 0.3 .mu.m is formed by exposing and developing the resist 8.

Detailed Description Text (10):
Then, the interlayer insulating film 7 is etched partially via the via opening portion 8a by the reactive ion etching (RIE) method by using the resist 8 as a mask, to thus form a via hole 9 of a diameter of 0.3 .mu.m, as shown in FIG. 3B.

Detailed Description Text (11):
In etching, the ICP plasma equipment (not shown) is employed. As etching conditions, C.sub.4 F.sub.8, CH.sub.2 F.sub.2, and Ar are introduced into the chamber at a flow rate of 15 sccm, 10 sccm, 150 sccm as the reaction gas respectively, the substrate temperature is set to 10.degree. C., the pressure in the chamber is set to 5 mTorr, the ICP supply power is set to 2000 W, the bias power is set to 900 W, and the etching time is set to 70 seconds.

Detailed Description Text (12):
Then the resist 8 is removed by the solvent, then the silicon substrate 1 is loaded into the chamber of the sputter etching equipment (not shown), and then an argon gas is generated in the low pressure atmosphere whose inner pressure is set to 0.5 mTorr. As shown in FIG. 3C, argon ions are irradiated to the interlayer insulating film 7 at an angle of 30 to 60 degrees, preferably almost 45 degree, relative to a perpendicular line to an upper surface of the silicon substrate 1. Thus, a corner of the interlayer insulating film 7 which defines an upper edge of the via hole 9 is cut off to thus form an inclined surface 9a. As a result, an upper area of the via hole 9 can be extended.

Detailed Description Text (18):
Then, as shown in FIG. 3E, the silicon substrate 1 is loaded in the pretreatment chamber of the cluster equipment employed to form the metal film, and then the substrate is annealed at 200 to 400.degree. C. in the atmosphere of 1 to 500 mTorr, into which hydrogen (H.sub.2) of 80 flow rate % and argon (Ar) of 20 flow rate % are introduced, so that the copper oxide formed on the surface of the wiring 5 can be removed. In place of this method, such a method may be employed that first the silicon substrate 1 is

loaded in the atmosphere of 1 to 500 mTorr, into which hydrogen (H.sub.2) of 80 flow rate % and argon (Ar) of 20 flow rate % are introduced, by using the ICP plasma equipment, and then the copper oxide formed on the surface of the wiring 5 is removed by reduction plasma. During above removal of the copper oxide, ammonia may be added to the gas.

Detailed Description Text (33):
A method of performing concurrently formation of the via-hole, removal of the resist, formation of the inclined surface on the upper portion of the via hole, and cleaning of the inside of the chamber, which are performed separately in the first embodiment, will be explained in the following.

Detailed Description Text (35):
Next, as shown in FIG. 4A, ashing of the resist 8 made of organic material is carried out by using the oxygen plasma, and at the same time the silicon nitride film 6 is physically etched by the argon contained in the plasma.

Detailed Description Text (38):
The interlayer insulating film 7 being exposed by removing the resist 8 is etched physically by the argon. Since this etching is isotropic etching, the upper edge portion of the interlayer insulating film 7 which defines the via hole 9 is etched. Thus, as shown in FIG. 4B, the upper edge portion of the via hole 9 is shaped as the inclined surface 9a. Since etching of the interlayer insulating film 7 is started after ashing of the resist 8 has been finished, merely the interlayer insulating film 7 is slightly etched.

Detailed Description Text (47):
According to another invention, since removal of the resist being employed in forming the hole or groove, and removal of the second insulating film via the hole or groove are executed simultaneously by using the oxygen containing plasma, the wiring is exposed to the oxygen plasma in the final stage of the etching of the second insulating film, so that the wiring becomes difficult to be oxidized because the surface of the second wiring is oxidized. As a result, sticking of the metal of the wiring onto the side wall can be prevented by suppressing the scattering of the metal from the wiring.

CLAIMS:

1. A semiconductor device manufacturing method comprising the steps of:

forming a wiring on a first insulating film which is formed on a semiconductor substrate;

forming a second insulating film for covering the wiring;

forming a third insulating film, which is made of material different from the second insulating film, on the second insulating film;

coating a resist on the third insulating film, and then forming an opening over the wiring by exposing and developing the resist;

forming a hole or groove in the third insulating film by etching the third insulating film via the opening with a reactive ion etching method;

removing the resist;

forming an inclined surface by etching an upper edge portion of the third insulating film around the hole or groove to thus extend an upper portion of the hole or groove;

after forming the inclined surface, removing a part of the second insulating film via the hole or groove by the reactive ion etching method; and

forming a metal film in the hole or groove.

9. A semiconductor device manufacturing method comprising the steps of:

forming a wiring on a first insulating film which is formed on a semiconductor substrate;

forming a second insulating film for covering the wiring;

forming a third insulating film, which is made of material different from the second insulating film, on the second insulating film;

coating a resist on the third insulating film, and then forming an opening over the wiring by exposing and developing the resist;

forming a hole or groove in the third insulating film by etching the third insulating film via the opening;

removing the resist by placing the semiconductor substrate in a plasma atmosphere containing oxygen in a chamber, and simultaneously removing a part of the second insulating film via the hole or groove to expose the wiring via the hole or groove; and

forming a metal film in the hole or groove.

11. A semiconductor device manufacturing method according to claim 9, wherein an inclined surface is formed by etching an upper edge of the third insulating film being exposed by removing the resist in the plasma atmosphere to thus extend an upper portion of the hole or groove.